Silicon Germanium CMOS Optoelectronic Switching Device: Bringing Light to Latch

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***Abstract*—We propose a novel semiconductor optoelectronic (OE) switch that is a fusion of a Ge optical detector and a Si metal–oxide–semiconductor (MOS) field-effect transistor (FET). The device operation principle is investigated, and the performance is explored by simulations. The proof of principle is demonstrated by experiments. The use of Ge enables operation in standard telecommunication wavelengths, in addition to providing the surrounding Si circuitry with noise immunity from signaling. The transconductance of the FET provides amplification, and an experimental current gain of up to 1000 is demonstrated. A complementary function is shown by tailoring the doping profiles. The circuit performance of a complementary pair using the International Technology Roadmap for Semiconductors values for the 150-nm node is evaluated by simulation, yielding ∼100-ps cycle times. The switch can be fabricated in the nanoscale regime along with a high-performance Si complementary MOS. A very low capacitance can be achieved due to the isolation of the detection region from the current drive. OE conversion that is performed with such a compact device offers the potential of inserting light at the latch level in a microprocessor.**

***Index Terms*—Germanium, integrated optoelectronics, metal–oxide–semiconductor field-effect transistor (MOSFET) switches, optical interconnections, optical logic devices, optical receivers, optoelectronic (OE) devices, photodetectors (PDs), photonic switching systems, silicon.**

I. Introduction

As THE speed of electronic circuits approaches 10 Gb/s and beyond, the volume of chip-to-chip and on-chip communication skyrockets. Traditional copper wires are efficient at short distances, but they suffer excessive power dissipation and delay in global lines and cannot cope with the ever-growing bandwidth demand [1]. Moreover, with the microprocessors evolving toward multicore architectures, the requirements for increased bandwidth density further strain electrical interconnects [2]. The idea of bringing high-speed optical signals directly to a CMOS chip offers opportunities for using light to aid electrical functions in novel ways. This seems increasingly imminent, as optical interconnects are promising to alleviate the problems faced by copper wires [3]. Compound semiconductors have been the forerunner in optoelectronic (OE) applications, but their integration with Si is expensive and is hindered by parasitic effects. Recently, it has been demonstrated that the incorporation of Ge into Si is a promising approach that can enable the design of low-cost modulators [4] and optical detectors [5], [6] on Si with potentially higher efficiencies than their hybrid counterparts. This technology is fast becoming a replacement for the conventional building blocks of the transmitter end in an optical link operating at telecommunication standard wavelengths.

Traditional optical receivers are composed of a photodetector (PD) that feeds a transimpedance amplifier stage, which converts the electrical current from the PD into a voltage signal. This voltage signal is then amplified by a cascade of buffer and amplifier stages. Subsequently, the signal is used to drive the next-stage logic, where it was initially intended. Inevitably, this scheme generates a huge overhead in power consumption and chip real estate; hence, it poses a serious scalability problem for large-scale integration. Moreover, increasingly stringent power requirements on a chip limit the total number of receivers and, hence, the total number of links. Some research has focused on eliminating the bulky receiver circuitry and replacing it with back-to-back PDs [7]. A successful operation has been demonstrated with such totem-pole configuration with < 6-ps rms jitter. This scheme, on the other hand, requires two consecutive optical signals that are precisely separated in time to arrive at the PDs throughout the chip.

The influence of detector capacitance on the system-level performance of optical interconnects was recently analyzed by Cho *et al.* for chip-to-chip links [8]. As the capacitance of the PD is reduced, optical links become more power efficient than their electrical counterparts. Haurylau *et al.* have reported similar findings for on-chip interconnects [9]. It is imperative to lower the detector capacitance in facilitating the insertion of optical interconnects into the very large scale integration domain.

In this paper, we introduce a novel OE switch for chip-to-chip and on-chip optical signaling and clocking applications. The building block for the switch is an OE MOSFET. The proposed device scales with the technology and can be made to be extremely compact with very low capacitance and small footprint area. By such a design, light can be introduced at the latch level, eliminating the ever so power-hungry electrical interconnection hierarchy of clock distribution networks, as well as the conventional high-capacitance optical detectors for optical interconnects.

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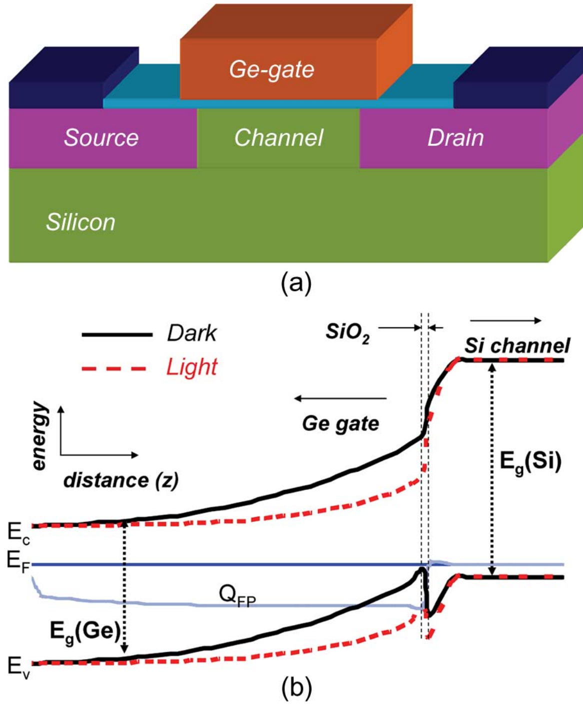


Fig. 1. (a) Schematic of a cross section of the OE MOSFET. The source–drain and channel regions are formed in Si. The Ge gate is deposited and isolated from the channel by thermally grown SiO_2. Light can be coupled by normal incidence or by a through-waveguide scheme. The light in the 1.3–1.55 μm window is absorbed in the Ge gate only. Due to the large band gap energy of Si, no absorption takes place in the channel; hence, the surrounding Si circuit is immune to noise. (b) Energy band diagram of the Ge–SiO_2–Si stack. Band bending under equilibrium and steady-state illumination is shown by the solid and dotted lines, respectively. Optically generated carriers accumulate at either side of the gate dielectric. This photoexcited charge modifies the electric field across the stack. In the case illustrated here, holes accumulate at the Ge–SiO_2 interface, whereas the electrons are swept toward the SiO_2–Si interface, inducing a channel.

II. Device Description and Operation

A. Device Structure

The schematic of the structure of the proposed device is shown in Fig. 1(a). It is a conventional Si MOSFET with an absorption region at the gate of the transistor. The channel of the OE MOSFET is Si, while the gate is Ge. The source and drain regions are formed by conventional doping of the Si body. In short, the device is a Si MOSFET with a Ge gate. Light can be coupled into the device from the top surface, as well as through a waveguide in a fully integrated scheme.

B. Principle of Operation

The signal is generated externally and is transmitted in the form of optical energy in the 1330–1550-nm window, where Ge is a strong absorber. Incoming photons are absorbed only in the Ge gate, because Si is transparent at these wavelengths. The absorbed photons generate electron–hole pairs in the gate. Optically generated carriers then move within the gate in an electric field caused by band bending and the applied gate bias, as shown in Fig. 1(b). In the case illustrated in this figure, the optically generated electrons drift away from the SiO_2 interface, whereas the holes drift toward this interface. This constitutes a net current in the gate terminal I_{GATE}, resulting in the accumulation of electrons and holes at opposite sides of the gate insulator. Consequently, the external electric field is suppressed by the electric field due to the optically generated charge buildup. The band bending and the quasi-Fermi levels for electrons Q_{fn} and holes Q_{fp} are modified, owing to the new charge distribution, as indicated by the dashed lines in Fig. 1(b). Therefore, the electric field in the gate is reduced while the potential across the gate oxide and the channel increase. This behaves like a gate voltage, so the drain-to-source current can be modulated as an amplified version of the gate current with the increased carrier density in the channel. When the light is turned off, the gate oxide capacitance discharges through both the increased recombination in the gate depletion region and the diffusion due to the gradient in the carrier concentration. The speed of the turn-off mechanism can be controlled by the carrier lifetimes and the thickness of the gate region, as well as the applied gate bias. Furthermore, it is possible to tailor the built-in band bending using a graded SiGe gate region. Owing to the unique band offsets between Si and Ge, the valence band can be engineered for a more efficient removal of excess carriers.

In this device, the absorbing Ge gate and the Si FET regions are electrically isolated by a high-quality insulator, such as a thermally grown SiO_2. The electrical current from the FET is modulated, not by the optically generated carriers but by the electric field due to these carriers. Furthermore, the band gap energy of the Ge absorption region is lower than that of the Si FET regions. Therefore, there is no significant optical generation of carriers in the Si channel when light enters the body of the transistor. In a classical optical FET, however, the channel is illuminated directly, and photoexcited carriers are generated in the channel. The diffusion of these carriers limits the speed of the device. Moreover, the surrounding Si transistors would suffer from light-induced noise generation. On the contrary, in this device, a high-speed optical-to-electrical conversion is possible while the surrounding Si circuitry is noise free, providing noise immunity from signaling and clocking.

C. MOS Capacitor

An alternative way to model the operation of the device is to consider the capacitive voltage division in the Ge–SiO_2–Si gate stack, which governs the operation of the device. Three capacitors in series connection—gate depletion C_{Ge}, insulator C_{ox}, and channel depletion C_{Si}—divide the potential difference across the gate stack. The equivalent capacitance C_{TOTAL} of the capacitors in series is given by

$$\frac{1}{C_{\mathrm{TOTAL}}} = \frac{1}{C_{\mathrm{Ge}}} + \frac{1}{C_{\mathrm{ox}}} + \frac{1}{C_{\mathrm{Si}}}. \tag{1}$$

The value of the equivalent capacitance is dominated by the smallest capacitance among the three. MEDICI was used for 2-D electrostatic and transient device simulations to analyze the gate stack. The simulated structure is a stack of 300-nm Ge with 10^{18} cm^{-3} p-type doping and 5-nm SiO_2 on p-type Si with 10^{16} cm^{-3} doping concentration. C_{TOTAL} versus gate

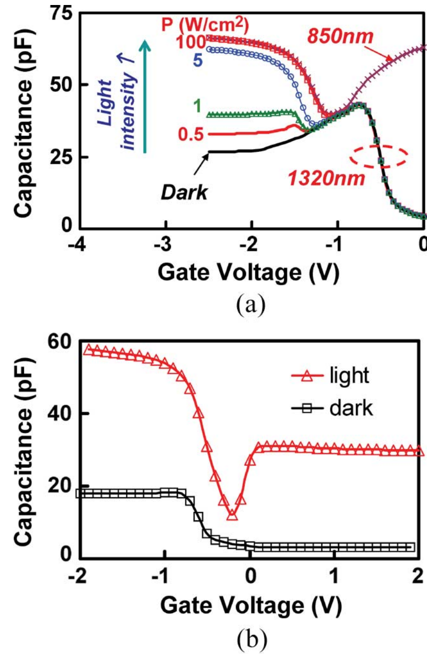


Fig. 2. (a) Capacitance of the Ge–SiO_2–Si stack simulated with varying light intensities and gate voltages. Si does not absorb 1320-nm light, so only Ge depletion capacitance is modulated at $\lambda = 1320$ nm. A single curve is shown at $\lambda = 850$. Both Si and Ge absorb at this wavelength; hence, Si depletion capacitance is also modulated with 850 nm. (b) Measured high-frequency (100 kHz) $C_{\mathrm{GATE}}-V_{\mathrm{GATE}}$ curves for 3.5-nm-thick SiO_2. Due to experimental difficulties, a visible microscope light is used in the measurements. Si also absorbs at this wavelength; hence, Si depletion capacitance, which is dominant when $V_{\mathrm{GATE}} < 0$, is also modulated.

voltage V_{GATE} curves with varying light intensities are plotted in Fig. 2(a). For $V_{\mathrm{GATE}} < -1$ V, the Si channel is accumulated; hence, C_{TOTAL} is equivalent to the series connection of C_{Ge} and C_{ox}. Incident light with $\lambda = 1320$ nm is absorbed in the Ge gate, increasing the stored charge and, hence, increasing C_{Ge}. The film thicknesses are given such that $C_{\mathrm{ox}} \gg C_{\mathrm{Ge}}$, so C_{TOTAL} increases with increasing C_{Ge}. The capacitance is modified by light, because the optically generated carriers in the gate depletion region act as an extra source of charge. Due to capacitance change, $Q_{\mathrm{inversion}}$ is also modulated with the incoming light.

When $V_{\mathrm{GATE}} > -1$ V, Si is depleted and finally inverted, while the gate is accumulated. Since the Ge region is in accumulation, C_{TOTAL} is equivalent to the series connection of C_{Si} and C_{ox} and cannot be modulated by the absorption in the gate. Moreover, Si is transparent at $\lambda = 1320$ nm, so C_{TOTAL} is unchanged with the incoming light at this wavelength. A single curve is plotted for incident light with $\lambda = 850$ nm, which is absorbed by both Si and Ge. C_{TOTAL} increases with C_{Si} as the stored charge increases due to absorption in the Si depletion region.

III. Device Fabrication

To verify the simulation results, we fabricated Ge–SiO_2–Si structures. The starting substrates were (100)-oriented p-type ($\sim 10^{15}$ cm^{-3}) Si wafers, which were cleaned by standard organic and metal cleans, followed by a 30-s hydrofluoric acid dip to remove chemical oxide on the surface. A 3.5-nm-thick SiO_2 layer was thermally grown at 900 °C, followed by 240-nm polycrystalline Ge deposition. No intentional impurity was introduced during or following the Ge deposition. The gate regions were patterned by photolithography and dry etched. Finally, the samples were annealed at 400 °C in a forming gas ambient for 45 min. Fig. 2(b) plots the measurement results showing the measured capacitance changing with light, as predicted by the simulations. Due to experimental difficulties, visible light was used in the capacitance measurements. When $V_{\mathrm{GATE}} < -1$ V, the Si channel is accumulated while the Ge gate is inverted. In this region, the total capacitance C_{TOTAL} is roughly equal to C_{Ge}, because C_{ox} is considerably high. The light absorbed in the space charge region modifies the depletion width in the gate. This modulates C_{TOTAL} and, hence, the stored charge. The accumulation and inversion conditions for Si and Ge are swapped when $V_{\mathrm{GATE}} > 0$ V. Similarly, the equivalent capacitance is now dominated by C_{Si}, and the light absorbed in the channel modifies C_{TOTAL}.

The OE MOSFETs were fabricated on (100)-oriented p-type ($\sim 10^{15}$ cm^{-3}) Si substrates. The wafers were initially cleaned by standard clean (SC): 10 min in 4 : 1 $H_2SO_4 : H_2O_2$ and 10 min in 5 : 1 : 1 $H_2O : H_2O_2 : HCl$ to remove organics and trace metals, respectively. Following the SC, the wafers were dipped in 50 : 1 $H_2O : HF$ for 30 s to remove the chemical oxide that formed on the surface of Si. Immediately after the HF clean, the wafers were loaded into the oxidation furnace to grow 500 nm of SiO_2 at 1000 °C in steam ambient. This growth was sandwiched between two steps of high-quality thin SiO_2 grown in dry ambient within the same atmospheric furnace. This oxide layer is used as a field isolation of individual MOSFETs. In order to define active areas for the devices, the field oxide was then patterned by photolithography, followed by wet etching in 6 : 1 $H_2O : HF$ buffered oxide etchant. The photoresist was removed by hot sulfuric acid, and the wafers were again cleaned by SC, followed by a 30-s HF dip. A 40-nm sacrificial SiO_2 layer was thermally grown in order to reduce the ion implant damage to the surface and to avoid dopant outgassing during subsequent annealing steps. The samples were then doped with boron. A double implant was performed: The first was with a 180-keV B11 with a dose of 5×10^{12} cm^{-2} to form a p-well, and the second was with a more shallow 50-keV B11 with a dose of 1.4×10^{12} cm^{-2} to adjust the threshold voltage. The samples were cleaned by SC, following the ion implantation, and annealed for 1 h in inert ambient at 1000 °C in order to diffuse and activate the doped regions.

The wafers were then implanted by 100-keV 5×10^{15} cm^{-2} As75 using photoresist as the masking layer, followed by source–drain anneals for 15 min at 1000 °C in N_2 ambient. The wafers were then cleaned with SC, this time followed by a longer 50 : 1 HF to remove the sacrificial oxide. Immediately after the sacrificial oxide strip, 5.7-nm high-quality SiO_2 was grown as the gate oxide at 900 °C in dry ambient, followed by 240-nm germanium gate deposition at 450 °C. Ge deposition on SiO_2 is challenging, because the reactions favor SiO_2 being removed, instead of Ge being deposited [10]. Therefore, a very thin (< 20 Å) layer of Si "seeding" layer was deposited preceding the Ge film. It is difficult to remove contaminants

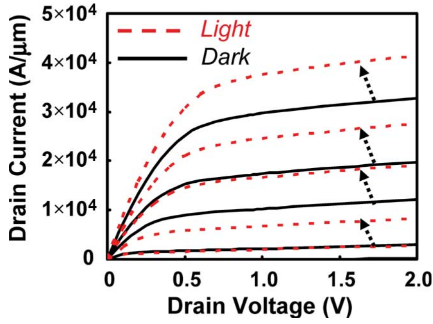


Fig. 3. Simulated $I_{\rm DRAIN}-V_{\rm DRAIN}$ results of a 1-μm-gate-length transistor with n-doped Ge (10^{16} cm^{-3}) and p-doped Si (10^{18} cm^{-3}). Incident light (1 μW/μm^2, in this case) constitutes a gate signal.

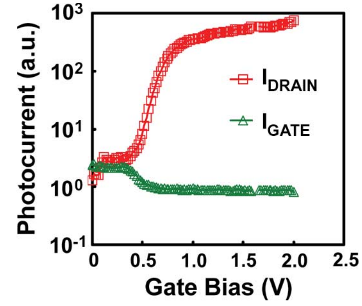


Fig. 4. Measured photocurrent at the gate and drain terminals when $V_{\rm GATE} = V_{\rm DRAIN}$. The flow of optically generated carriers in the gate constitutes gate current $I_{\rm GATE}$, which is amplified by the transconductance of the FET at the drain terminal $I_{\rm DRAIN}$. The lock-in technique was used to precisely extract the optical currents.

from the Ge surface, so the Ge film was capped with a thin (< 40 nm) low-temperature oxide (LTO) layer immediately after deposition. Various techniques have been demonstrated to obtain single-crystal Ge on SiO_2, such as lateral overgrowth (necking) [11], [12], rapid melt crystallization [13], [14], and metal-induced crystallization [15]. The crystallinity of the Ge layer will affect the lifetime of the optically generated carriers and hence will influence the overall sensitivity and the speed of the device. In this experiment, polycrystalline Ge is used for the proof of concept, owing to its relative ease of deposition.

Transistors with gate lengths L_G and widths W_G ranging from 1–100 μm were patterned by photolithography and etched by reactive ion etching to achieve straight side walls. A 280-nm-thick LTO layer was deposited to protect the surface. Via holes were opened into the LTO layer, followed by a 250-nm Al deposition. A thin layer of Ti (< 20 nm) was deposited first, as a barrier against Al diffusion into Si and Ge. The aluminum film was patterned and etched to form the electrical probing pads. Finally, the samples were annealed at 400 °C in a forming gas ambient for 45 min.

IV. Device Characterization

Typical $I_{\rm DRAIN}-V_{\rm DRAIN}$ results obtained by MEDICI simulations are shown in Fig. 3. The plotted characteristics are for a transistor with $L_G = 1$ μm that is formed on p-type Si with an acceptor concentration of 10^{18} cm^{-3} and on n-type Ge gate with a donor concentration of 10^{16} cm^{-3}. $I_{\rm DRAIN}$ values are shown with and without optical illumination of 1-μW/μm^2 intensity. The $I-V$ characteristics of the OE MOSFET are comparable to those of a conventional Si MOSFET, regardless of whether light was an input. The incident light acts as an additional gate voltage bias modifying the conductivity of the Si channel.

The optical characteristics of the device were obtained using an internally modulated semiconductor laser at a wavelength of 1.55 μm. The laser output was coupled to a single-mode optical fiber. The light from the end of the fiber was irradiated onto the device via an optical setup such that the beam and the sample could be monitored simultaneously on an infrared camera. The light was coupled into the gate from the top surface. No attention was paid to antireflection coating, as this can be separately designed for improved coupling efficiency. There is no dc gate current (within the measurement noise limit) due to the insulating SiO_2 layer. A synchronized lock-in amplifier was used to precisely extract the photocurrent component of the measured signal. Fig. 4 plots the measured optical gate and drain currents versus the gate voltage for $V_{\rm GATE} = V_{\rm DRAIN}$. The measured drain current is up to three orders of magnitude larger than the gate current, which can be attributed to the built-in gain of the transistor. The measured responsivity of the device is less than the simulation estimates, which is potentially attributed to the high recombination rates in the Ge gate due to the polycrystalline nature of the deposited Ge film. The increased recombination at the gate significantly limits the sensitivity.

The response speed of the OE MOSFET is limited by the FET cutoff frequency $f_{\rm cutoff}$, the drift speed of the photogenerated carriers in the absorption region, and the RC time constant of the absorption region. The FET cutoff frequency is determined by the gate length and the carrier mobility in the channel. To increase $f_{\rm cutoff}$, it is necessary to shorten the length of the FET channel and to use high-mobility material for the channel. The RC time constant is determined by the dimension of the absorption region and the lifetime of carriers. By reducing the dimension of the absorption region, the RC time constant will be decreased, and the cutoff frequency will be increased. When the channel is long, the overall cutoff frequency is determined by $f_{\rm cutoff}$. When the length of the channel is shortened, the drift velocity or the RC time constants limit the cutoff frequency.

The intrinsic speed of the device is obtained by impulse response simulations. Ge is assumed to be of a single crystal in the simulations, because there are no existing models for the polycrystalline grain boundaries. The grain boundary influence is predicted to reduce the carrier lifetime, thus further increasing the device speed, trading off with sensitivity. The intrinsic speed increases with the shrinking gate length. The calculated full-width at half-maximum from impulse response simulations are < 1 ns and < 100 ps for $L_G = 1$ μm and $L_G = 100$ nm, respectively. The high-speed performance of the OE MOSFET is benchmarked against that of a traditional PD. The response of a classical metal–semiconductor–metal (MSM) PD to a train of optical pulses is plotted in Fig. 5. The simulated MSM has a 100-nm electrode spacing on a 100-nm-thick Ge layer.

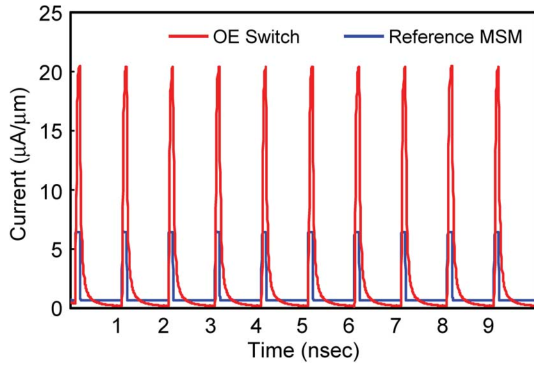


Fig. 5. Simulated transient response comparing a classical detector and the proposed device. The input is a pulse train, with each pulse delivering 1-fJ optical energy. The OE MOSFET has significantly enhanced responsivity and lower OFF-state leakage.

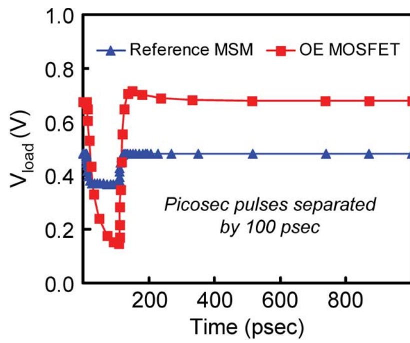
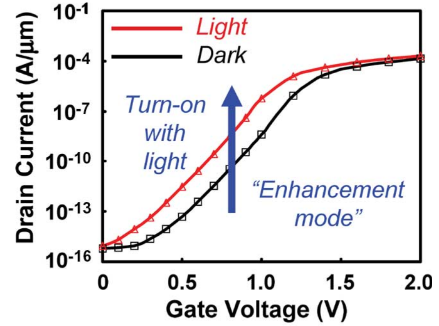


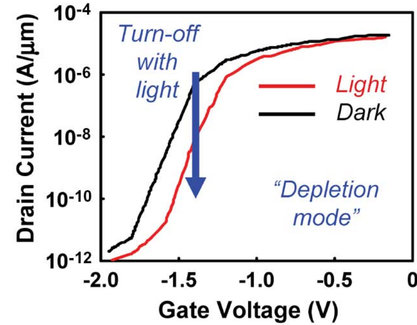
Fig. 6. Simulated optical transient response of totem-pole-connected MSM with OE MOSFET. In each case, the input is two short optical pulses that are delayed by 100 ps and deliver 10^{-17} J optical energy. The OE MOSFET provides $> 4\times$ voltage swing with identical input optical energies, driving similar capacitors.

In comparison, the transient response obtained from the OE MOSFET with identical 100×100 nm slabs of Ge in the gate is also plotted in Fig. 5. This device provides a significantly higher photocurrent ($\sim 3.5\times$) for identical optical energies, in addition to lower OFF-state leakage ($\sim 4\times$). However, the relatively long tail can limit the maximum frequency and should be taken into account for further analysis, including noise performance. The output capacitance of the device C_{switch} is dominated by the gate-to-drain overlap, and it is $\sim$0.02 fF for an OE MOSFET with 100-nm gate length and width. Therefore, the RC-limited bandwidth is very large.

Another scheme that we employed to compare the performance of the proposed device is the totem-pole-style [7] receiverless operation. The simulated response from two back-to-back MSM detectors driving a capacitance (0.5 fF in the 150-nm technology node [16]) is plotted in Fig. 6, together with that from two OE MOSFETs that are connected in a similar fashion and driving an identical capacitance. Two short pulses that carry 10^{-17} J each and are delayed in time by 100 ps are incident in both cases. The OE MOSFET provides a significantly higher voltage swing with the same input optical energy. This essentially means that less number of post amplification stages are required to raise the voltage level to the logic rail, reducing excess power dissipation, delay, and area.



(a)



(b)

Fig. 7. (a) Simulated $I_{\mathrm{DRAIN}}-V_{\mathrm{GATE}}$ results show the effective gate signaling by incoming light. The device is normally off and turns on when illuminated with light, hence the "enhancement-mode" switch. (b) $I_{\mathrm{DRAIN}}-V_{\mathrm{GATE}}$ characteristics of a device that is normally on. When illuminated, the device turns off (depletion mode). Gate and channel doping types are switched to achieve this behavior: p-doped Ge (10^{16} cm^{-3}) and n-doped Si (10^{18} cm^{-3}).

The proposed device essentially is an optical detector with a built-in gain mechanism. In comparison, avalanche photodiodes (APDs), for instance, provide gain by impact ionization. However, APDs require high bias voltages (20 V/μm) to achieve the desired ionization rates, which is an increasingly difficult challenge to meet at the operating temperatures of today's high-end processors. In contrast, the OE switch allows low-voltage operation that is suitable for on-chip applications and a potentially better noise performance due to the separation of absorbing and conduction regions.

V. Complementary Operation

A. *More Light, Less Conduction*

Unlike classical optical receivers, a complementary operation is also attainable by this device scheme. The doping in the Ge gate and Si channel regions can be tailored such that the MOSFET drain-to-source current is reduced with the incident light. In other words, it is possible to configure a device that becomes less conductive as it absorbs more light. Such a device would be similar to a *depletion-mode* MOSFET [or p-channel (p-MOSFET)] and presents a complementary function to the enhancement-mode operation [or n-channel MOSFET (n-MOSFET)]. To demonstrate this concept, a depletion-mode device with $L_G = 1$ μm channel was simulated on n-type Si with an acceptor concentration of 10^{18} cm^{-3} and p-type Ge gate with a donor concentration of 10^{16} cm^{-3}. Fig. 7 compares the $I_{\mathrm{DRAIN}}-V_{\mathrm{GATE}}$ characteristics of the

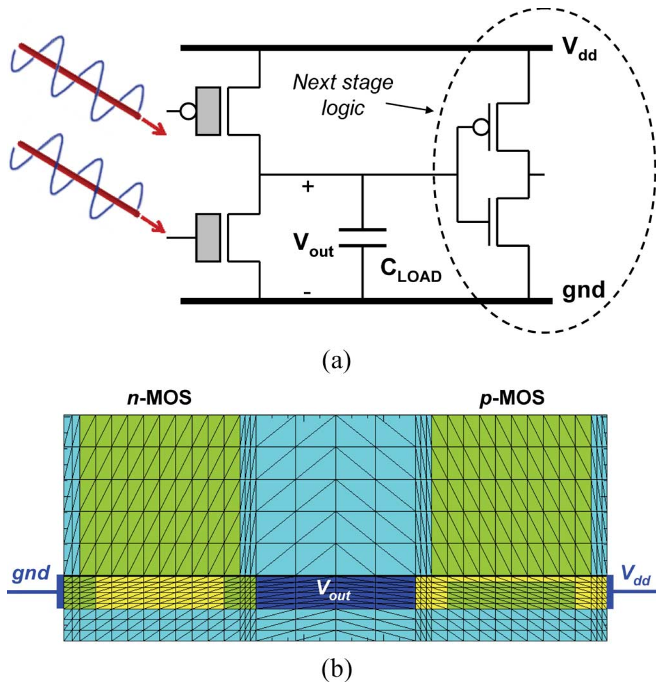


Fig. 8. (a) Complementary optical MOSFET pair connected as an inverter. The next stage is represented with a load capacitor. The capacitance is equal to that of a minimum-sized inverter in 150-nm technology node. (b) Simulation mesh structure of the complementary pair forming an optically controlled electronic inverter.

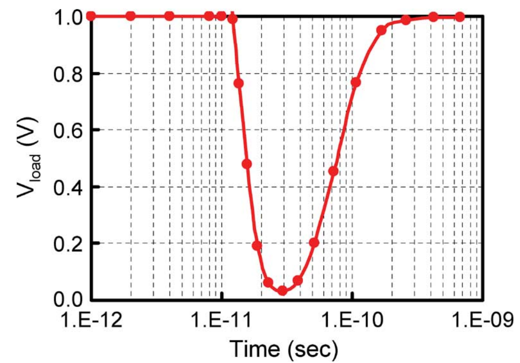


Fig. 9. Simulated transient response of the complementary optical MOSFET pair. The optically controlled electronic inverter is driving a minimum-sized inverter as the next stage. The light pulse arrives at 10 ps. The output voltage is plotted in time. It is possible to achieve a very fast rail-to-rail swing even with no amplification stages. Family curves are plotted with changing dc gate bias.

"enhancement mode" and "depletion mode" of operation with and without light. The enhancement-mode device turns on with incident light, as described in Section IV. The depletion-mode device, however, is normally on and turns off when illuminated with light. The OE n-MOSFET and p-MOSFET devices can be connected as a CMOS inverter to create an OE latch with light as the input signal.

B. Optically Controlled Electrical Inverter: Paving the Way to Bring Light to Latch

The arrangement, as described in Section V-A, is illustrated in Fig. 8(a), in which, an optical signal irradiates the pair of complementary OE MOSFETs. The pair then drives the next-stage logic, which is represented by gate capacitance C_{LOAD}. The characteristics for the optically controlled electrical inverter are obtained by MEDICI transient device and circuit simulations. The simulated structure and mesh are shown in Fig. 8(b). No accurate models exist for polycrystalline Ge, so the gate is assumed to be crystalline Ge during the simulations. The channel lengths are chosen to construct a minimum-size inverter in the 150-nm technology node [16]. For circuit operation, it is desirable to design the channel widths of the n-MOSFET and p-MOSFET independently. However, MEDICI is a 2-D simulator, so the channel widths are assumed to be identical. The next-stage logic is chosen to be a minimum-size inverter, which is one of the building blocks of the electrical logic, in the same technology node. When there is no optical input, the p-MOSFET is turned on, whereas the n-MOSFET is off. The output capacitor is charged up to V_{dd}; hence, it is at the logic-HIGH state. This could be considered as the initial condition. The input optical signal is a short pulse that excites the pair of complementary OE MOSFETs simultaneously. Upon arrival, the optical pulse turns the n-MOSFET on and the p-MOSFET off. The next-stage logic gate is discharged through the n-MOSFET during the optical pulse, pulling the output voltage down to the logic-LOW state. As the photoexcited carriers are removed, the pair recovers to the initial state, charging C_{LOAD} back to V_{dd}. Therefore, an electrical 1-to-0 transition, followed by a 0-to-1 logic transition, is attained with the incident optical pulse. The simulated temporal response of the optically controlled inverter is shown in Fig. 9, which plots output voltage V_{LOAD} versus time. The speed of output-high-to-low transition is on the order of 10–20 ps and depends strongly on the thickness of the absorbing layer. The width of the electrical pulse is determined by the low-to-high transition, which is governed by the RC time in the absorbing layer. Switching times of as short as 100 ps are achieved, corresponding to bit rates of $\sim$10 Gb/s. This could be further improved by designing a thinner absorbing region with shorter carrier lifetimes (such as in polycrystalline germanium), with the tradeoff of reduced sensitivity. As previously mentioned, the p-MOSFET and n-MOSFET channel widths can be independently tailored to "match" the complementary couple. In other words, by designing the relative channel widths, the pull-up and pull-down strengths of the pair can be balanced. Furthermore, the transistor channels can be scaled down for faster speeds.

C. Nanometallic Light Concentrators

Nanometallic structures can be used to concentrate optical energy to a very small scale, exploiting surface plasmonic waves. Experimentally, a factor of 5× enhancement in optical absorption has been demonstrated in [17], and in principle, it is possible to further increase this factor. The performance of the OE switch can be improved by concentrating light on such small dimensions as the gate of the optical MOSFET pair. The switching speed can be increased by shrinking the thickness of

the absorbing layer. Moreover, by squeezing more light into the volume of the absorbing gate region, the required optical energy for switching at a particular frequency could be reduced.

VI. Conclusion

We have introduced a SiGe switching device that can perform OE conversion in the nanoscale regime. The OE MOSFET exhibits gain, owing to a secondary photoconductive effect based on the current amplification of the FET. The switch is composed of a pair of complementary optical MOSFETs. The operation principle of the individual optical MOSFET is demonstrated by proof-of-concept experiments. The circuit performance of the complementary pair connected in an inverter fashion is investigated across various design parameters. Simulations show that it is possible for devices that are designed in the International Technology Roadmap for Semiconductors 150-nm technology node to achieve 100-ps cycling times. The switching device can be fabricated along with deeply scaled conventional MOSFETs using advanced Si technology. Such a device is extremely compact and has very small capacitance. This is particularly promising for on-chip clocking applications, which require a synchronizing signal to be distributed to a large number of nodes. This scheme promises OE conversion at the latch level, facilitating optical clock distribution on the chip. This eliminates the power dissipation and area due to electrical H-tree networks. Plasmonic coupling could be used to concentrate light on such dimensions by using nanometallic structures to further enhance device performance.

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